

CANmodule-II

Description

The CANmodule-II is part of Inicore's IPmodule family. The controller area network (CAN) bus, originally developed for the car industry, is a fast, reliable and cost-effective data bus for multi-master and real-time applications. In addition to automotive applications, it is in wide use in applications such as factory automation, machine control, building automation, maritime, medical, railway and avionics.

CANmodule-II is a full functional CAN controller that contains advanced message filtering, a transmit buffer with built-in priority arbiter and a receive message FIFO. With advanced message filtering capabilities, this core helps to off-load the CPU.

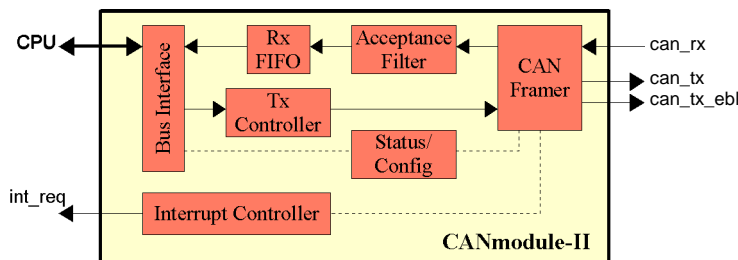


Figure 1: Block diagram

There are three independent acceptance filters with their own code and mask registers. Each filter covers the entire ID, IDE, RTR, and enhanced DeviceNet support, the first two Data fields. The four message deep receive FIFO contains the entire message including acceptance filter match indicators.

Three separate transmit buffers are available. To avoid priority inversion (e.g., a low priority message is sent before a high priority message), the transmit buffer contains a local message priority arbiter.

The CAN framer contains the complete data link layer, including the framer, transmit and receive control, error handling, error reporting and bit synchronization.

Features

- Full CAN2.0B compliant
- Maximum baudrate 1Mbps
- 3 acceptance filters for ID, IDE, RTR and 2 Data fields
- Enhanced for DeviceNet
- 3 Tx message buffers with priority arbitration
- 4 message deep Rx FIFO
- Local interrupt controller
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Register based design
- Full synchronous design
- Synthesis Options:
 - CPU readback enable
 - CPU bus width

Applications

- Factory automation
- Machine control
- Automotive
- Avionics and Aerospace
- Building automation

Utilization Table Optimized for Actel Devices

Family	Device - (speed grade)	Utilization				
		s-mod	c-mod	Tiles	RAM	Total
ProASIC ^{PLUS}	APA300			6542		80%
Axcelerator	AX500-3	1351	2467			47%
SXA	SX72A-3	1349	2670			67%

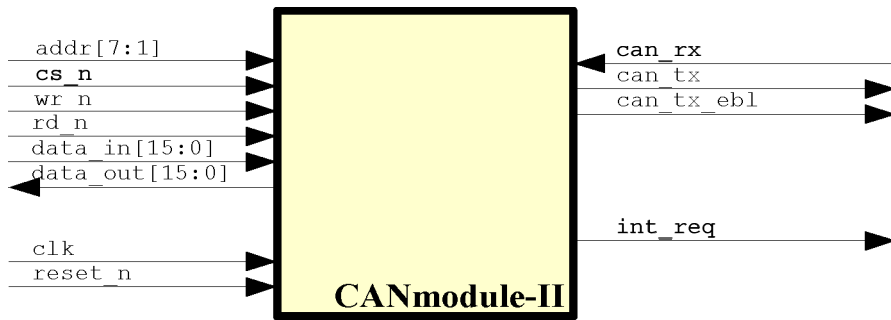


Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[7:1]	in	Address bus input
data_in[15:0]	in	Data bus input
data_out [15:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
int_req	out	Interrupt request
CANbus		
can_rx	out	CANbus receive signal from external driver
can_tx	in	CANbus transmit signal to external driver
can_tx_ebl	out	CANbus transmit enable for external driver

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. This core is also available with a SRAM based receive FIFO. For further information please review the CANmodule-IIr datasheet.

Using a separate APB wrapper, the core can be easily integrated into ARM based systems.

About Inicore

- ◆ FPGA and ASIC Design
- ◆ Easy-to-use IP Cores
- ◆ System-on-Chip Solutions
- ◆ Consulting Services
- ◆ ASIC to FPGA Migration
- ◆ Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

© 2002, Inicore Inc, All rights reserved.
All brands or product names mentioned are the property of their respective holders.

51205.71.01 Dec/2002