INI CORE

Datasheet

iniUART

Universal Asynchronous Receiver/Transmitter Core

Revision 2.0

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Revision History

Version	Date	Comments
2.0	07/11/2011	Global datasheet update

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1 Introduction

Inicore's iniUART is a versatile implementation of the Universal Asynchronous Receiver/Transmitter (UART) protocol. This core is designed as a building block for FPGA and ASIC implementation that need to interface with other serial devices.

The core contains a highly accurate baudrate generator, which allows to select any baudrate independently (up to 1/64) of the system clock speed. This means that there is no need for a fixed ratio between baudrate and system clock. The receiver uses three point input sampling and glitch rejection to increase noise immunity.

The iniUART supports 5, 6, 7, and 8 bit wide data characters, an optional parity (even or odd), and one or two stop bytes. The core does't contain any FIFOs making it an ideal candidate for low-level interface implementations or for application that require multiple ports.

1.1 Features

Following are the iniUART features:

- Single UART channel
- Very small
- Baudrate synthesizer for any baudrate of up to 1/64th of clock frequency
- 5, 6, 7, or 8 bit data format
- Parity enable, ddd or even
- Format and parity error detection
- 1 or 2 stop bits
- Three point input sampling and glitch rejection
- Parallel interface with event control
- Technology independent
- Fully synchronous design

1.2 Deliverables

- Netlist, VHDL RTL, or Verilog RTL source code
- Verification testbench
- Timing constraints file

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- Synthesis script
- User Guide

1.3 Block Diagram

The main building block and interface signals of the iniUART are shown in the block diagram below:

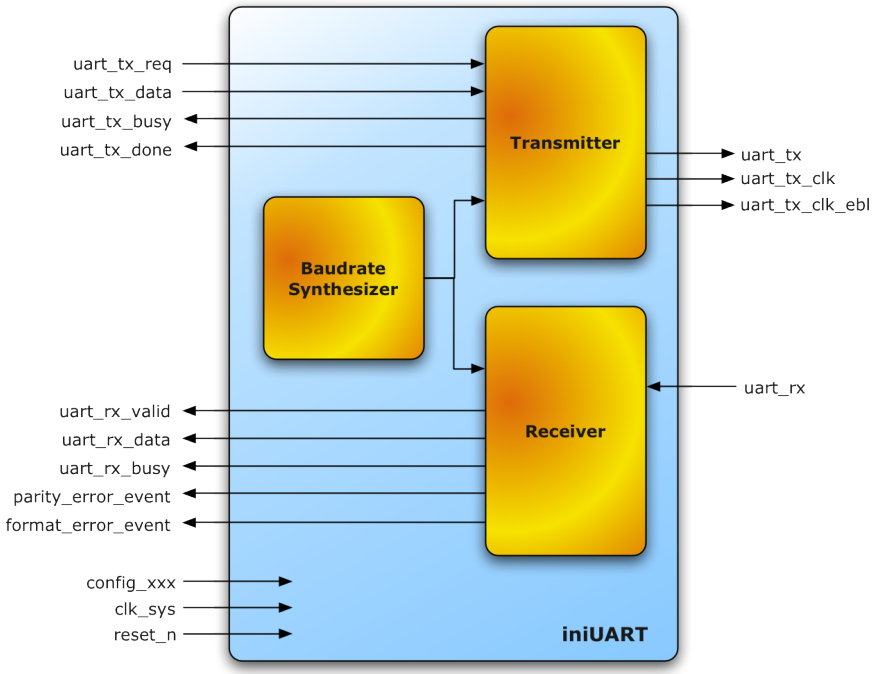

Figure 1: Block Diagram iniUART

1.4 Block Description

- Baudrate Synthesizer
  The baudrate generator is not a simple prescaler, but an innovative digitally controlled oscillator which allows generating any baudrate from the system clock. This makes system integration much easier as the common baudrate dependency on the system clock is eliminated.
- Receiver
  The receiver translates the serial uart_rx bit stream into the parallel format according to the selected configuration. Parity and format errors are detected and reported.

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- Transmitter
  The transmitter formats transmit data according to the selected configuration and performs the parallel to serial conversion to generate the uart_tx bit stream.

1.5 UART Character Format

The standard UART character format consist of one start bit, five to eight data bits, an optional parity bit, and one or two stop bits. An example with 8 data bits and one stop bit is shown in figure 2. As can be seen, the idle level of the bus is high, the start bit is low and the stop bit is high again. The data is sent with the least significant bit first.

Figure 2: 8-bit UART Character Format

Figure 3 shows the UART character format with two stop bits.

Figure 3: 8-bit UART character format with two stop bits

Figure 4 shows the UART character format for 7 data bits and one parity bit. The parity can be either even or odd. Even parity means that the number of ones in the data field plus the parity bit are even.

Figure 4: 7-bit UART character format with parity bit

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2 Signal Descriptions

The following paragraph lists the input and output ports of the iniUART.

2.1 I/O Ports

The figure below shows all I/Os of the iniUART.

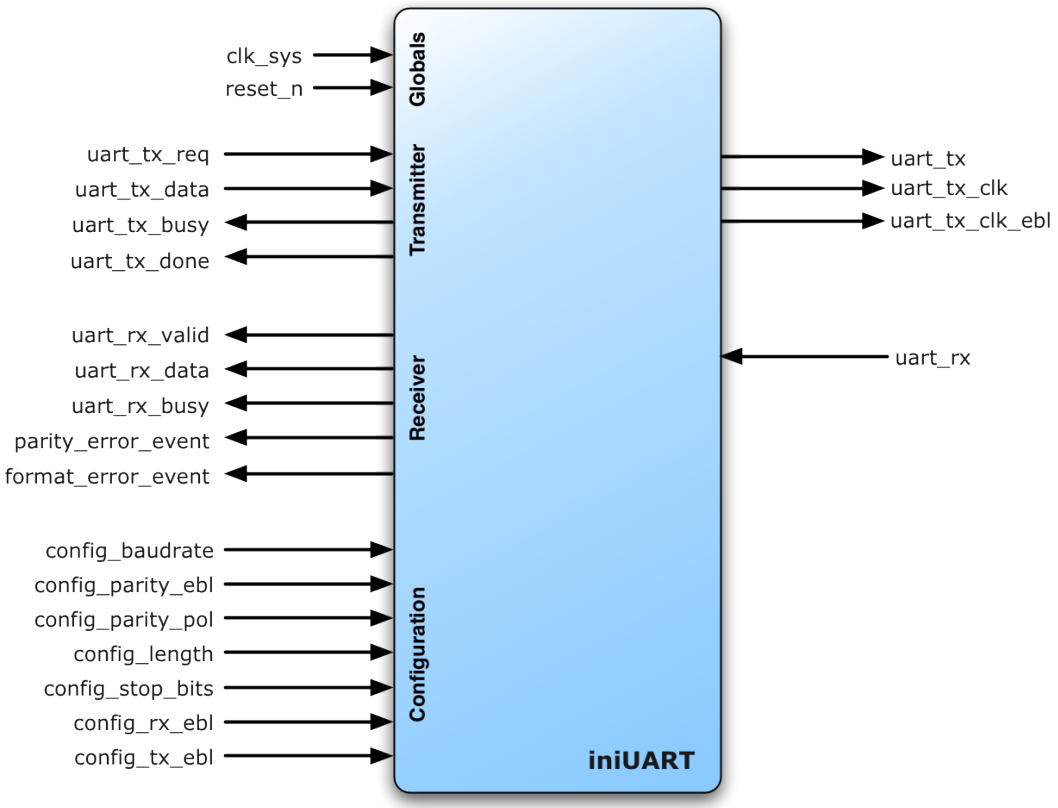

Figure 5: Symbol with I/Os

2.2 I/O Description

The following paragraphs list the inputs and outputs of the iniUART and provide an overview of the core's functionality.

2.2.1 Global Signals

All registers of this core are reset with the asynchronous active low reset_n. All registers are clocked with clk_sys. There are no other local clock or asynchronous reset signals.

Pin Name	Type	Description
reset_n	in	Asynchronous reset, active low
clk_sys	in	System clock

2.2.2 Configuration

The configuration signals are used to set the UART baudrate and the data format. All configuration signals are static inputs and may not be changed during operation.

Pin Name	Type	Description
config_baudrate[15:0]	in	Baudrate of serial data stream The receiver and the transmitter share the same baudrate generation. $config\_baudrate = \frac{2^{17}}{f_{clk\_sys}} 16 \cdot Baudrate$
config_length	in	Character length 0: 5-bit data field 1: 6-bit data field 2: 7-bit data field 3: 8-bit data field
config_parity_ebl	in	Parity enable 0: No parity field is used 1: Parity field is used

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Pin Name	Type	Description
config_parity_pol	in	Parity polarity 0: Even parity. The number of ones in data field including parity bit is even 1: Odd parity. The number of ones in data field including parity bit is odd
config_stop_bit	in	Length of stop bit field 0: Use one stop bit 1: Use two stop bits
config_rx_ebl	in	Receiver enable 0: Receiver is not enabled 1: Receiver is enabled
config_tx_ebl	in	Transmitter enable 0: Transmitter is not enabled 1: Transmitter is enabled

Baudrate Generator Configuration

The baudrate generator is not a simple prescaler, but an innovative digitally controlled oscillator which allows generating any baudrates from the system clock. There is no dedicated oscillator needed that is an exact multiple of the baudrate.

For configuring the baudrate, the 16-bit value is calculated according the following formula:

$$Baudrate = \frac{f_{clk\_sys}}{16}\frac{config\_baudrate}{2^{17}} \quad \textit{respective} \quad config\_baudrate = \frac{2^{17}}{f_{clk\_sys}} 16 \cdot Baudrate$$

where

Baudrate is the transmitting speed in bits per second
f_{clk_sys} is the system clock speed in Hz
config_baudrate is the 16-bit configuration value

Note:

- The maximal baudrate is 1/64th of the system clock frequency
- The lower the baudrate, the better is the accuracy.
- The higher the clock, the smaller is the edge jitter. Maximum absolute jitter is always equal $1/f_{clk\_sys}$

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2.2.3 Serial Interface

Pin Name	Type	Description
uart_tx	out	Transmit output pin
uart_rx	in	Receive input pin

2.3 Serial Bit Clocks

Synchronous to the serial bit stream uart_tx, a serial clock output is provided.

Pin Name	Type	Description
uart_tx_clk	out	Transmit Clock This clock is in phase with the uart_tx data stream. The rising edge is aligned with the beginning of a bit time.
uart_tx_clk_ebl	out	Transmit Clock Enable This clock enable is in phase with the uart_tx data stream. It is high for one clock cycle at the beginning of each bit time.

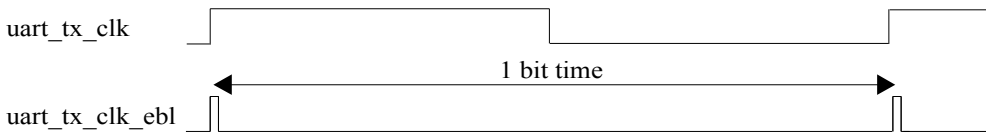

Figure 6: Serial Bit Clocks

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2.4 Transmitter Interface

The transmitter has a simple parallel user side interface.

Pin Name	Type	Description
uart_tx_data[7:0]	in	Transmit Data The transmit data is loaded into the transmit buffer when uart_tx_req is asserted. If the data length is less than 8 bits, the most significant bits are ignored.
uart_tx_req	in	Transmit data request Event for storing the tx_data in the transmit shift register and start of the transmission. It's up to the system to not activate this input when the iniUART is busy.
uart_tx_busy	out	Transmit Busy 1: The transmitter is busy sending the requested data 0: The transmitter is idle
uart_tx_done	out	Transmit Done A one clock cycle pulse indicates the end of the data transmission.

Figure 7 shows the timing diagram for transmitting data.

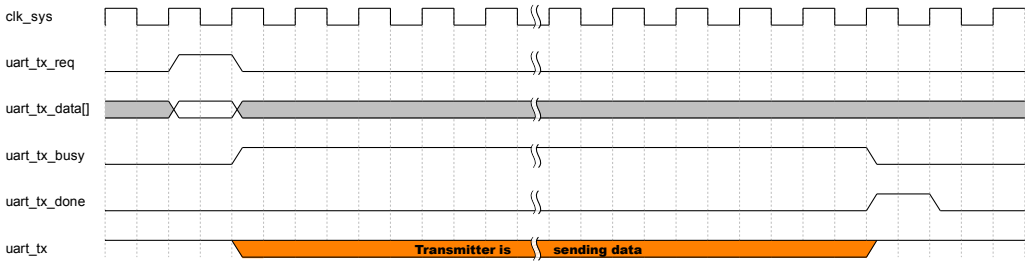

Figure 7: Transmitting Data

2.5 Receiver Interface

Pin Name	Type	Description
uart_rx_data[7:0]	in	Receive Data This is the captured data character. If the data length is less than 8 bits, the most significant bits are fixed at 0. uart_rx_data is only valid when uart_rx_valid is high.
uart_rx_valid	in	Receive Data Valid Event (active 1) for signaling that a byte has arrived and rx_data is valid now.
parity_error_event	out	Parity Error Event An active one event indicates that a parity bit error has been detected and the received characters aborted. This check is only performed when the parity feature is enabled (config_parity_ebl = 1).
format_error_event	out	Format Error Event An active one event indicates that a stop bit with the wrong level has been detected and the received characters aborted.

Figure 8 shows the timing diagram for receiving data:

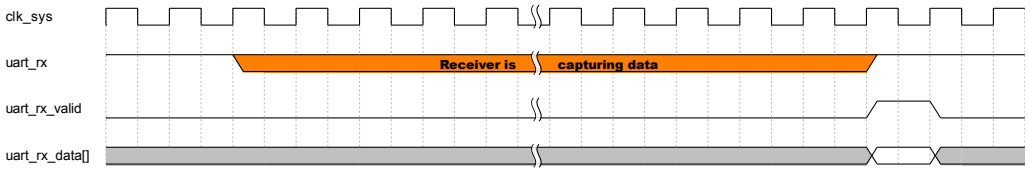

Figure 8: Receiving Correct Data

Figure 9 shows the timing diagram for receiving data where a parity error is detected:

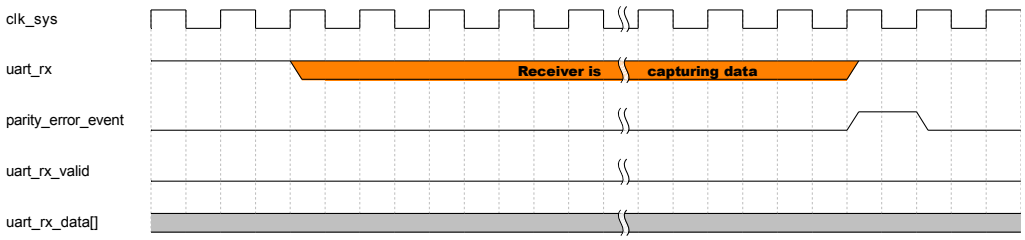

Figure 9: Receiving Data with Parity Error

About Inicore

- FPGA and ASIC Design
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- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

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