CANmodule-III

Version 2.2.5

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Definition of Terms

Following conventions are used in this document:

- CAN Data Order
  - CAN Data[63:56] is the 1st data byte of a CAN message
  - CAN Data[55:48] is the 2nd data byte of a CAN message
  - CAN Data[47:40] is the 3rd data byte of a CAN message
  - CAN Data[39:32] is the 4th data byte of a CAN message
  - CAN Data[31:24] is the 5th data byte of a CAN message
  - CAN Data[23:16] is the 6th data byte of a CAN message
  - CAN Data[15:8] is the 7th data byte of a CAN message
  - CAN Data[7:0] is the 8th data byte of a CAN message
- All default values are '0' unless otherwise noted
- Undefined bits in read back are read as '0'
- Following nomenclature is used register mapping
  - r : readback operation
  - R : Read operation
  - W : Write operation
- Signals ending with '_n' are active low

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Revision History

Version	*Comment*
2.2.5	· Error Status Registers are read only (page 18)
2.2.4	· tseg1 and tseg2, corrected bits assignments
2.2.3	· Corrected and refined Rx and Tx command and control buffer description
2.2.2	· ABP Bus address, bits assignment corrected (page 9)
2.2.1	· Refined description of operation · Updated signal names · Document restructured

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1 Overview

CANmodule-III is a full functional CAN controller module that supports the concept of mailboxes. It is compliant to the international CAN standard defined in ISO 11898-1.

It contains 16 receive buffers, each one with its own message filter, and 8 transmit buffers with prioritized arbitration scheme. For optimal support of Higher Level Protocols (HLP) such as DeviceNet or SDC, the message filter covers the first two data bytes as well.

The design is written in technology independent HDL and can be mapped to ASIC and FPGA architectures and makes use of on-chip SRAM structures. An AMBA Advanced Peripheral Bus (APB) interface enables smooth integration into ARM based SOC's. This full synchronous bus interface can easily be connect to other system buses.

1.1 Features

The CANmodule-III is designed for system-on-chip integrations.

Standard Compliant

- Full CAN 2.0B compliant
- Conforms to ISO 11898-1
- Maximum baudrate of 1 Mbps with 8 MHz system clock

Receive Path

- 16 receive buffers
- Each buffer has its own message filter
- Message filter covers: ID, IDE, RTR, Data byte 1 and Data byte 2
- Message buffers can be linked together to build a bigger message array
- Automatic remote transmission request (RTR) response handler

Transmit Path

- 8 Tx message holding registers with programmable priority arbitration
- Message abort command

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System Bus Interface

- AMBA 2.0 Advanced Peripheral Bus Interface
- Full synchronous zero wait-states interface
- 8, 16, or 32-bit wide data path
- Status and configuration interface

Programmable Interrupt Controller

- Local interrupt controller covering message and CAN error sources

Test and Debugging Support

- Listen only mode

SRAM Based Message Buffers

- Optimized for low gate-count implementation
- Single port, synchronous memory based
- 100% Synchronous Design

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1.2 Block Diagram

The main building blocks are shown in the following figure:

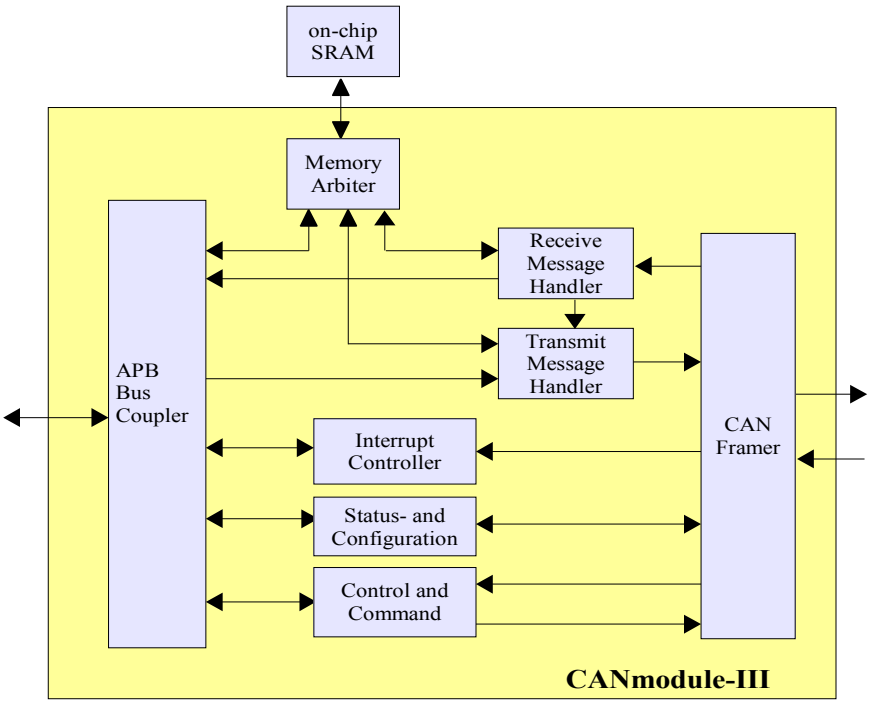

Figure 1: Block Diagram

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2 IO Description

The following paragraph lists the input and output ports of this core and explains their respective functionality.

2.1 Inputs – Outputs

This figure shows the main inputs and outputs.

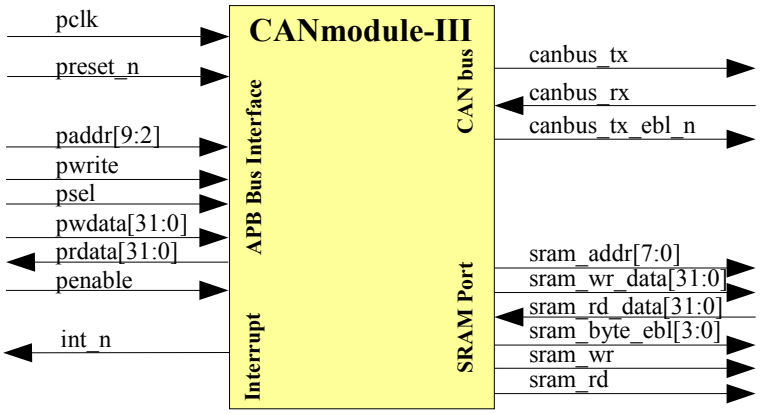

Figure 2: Inputs and Outputs

2.2 General Inputs

These pins are used to clock and initialize the whole core. There are no internally generated clocks or resets.

Pin Name	*Type*	*Description*
pclk	in	System clock
preset_n	in	Asynchronous system reset, active low

2.3 APB Bus Interface

The on-chip bus interface is compliant to the AMBA 2.0 APB bus specification. The interface is full synchronous to the system clock. The interface supports true 32-bit operation. 8-bit and 16-bit access are supported through separate top-level modules.

Pin Name	*Type*	*Description*
psel	in	Module select signal
penable	in	Bus transfer enable signal
paddr[9:2]	in	Address bus
pwrite	in	Read/write signal '0': read operation '1': write operation
pwdata[31:0]	in	Write data bus
prdata[31:0]	out	Read data bus
int_n	out	Interrupt request, active low

2.4 CAN Bus Interface

Three signals are provided to directly connect to a CANbus transceiver.

Pin Name	*Type*	*Description*
canbus_rx	in	Local receive signal (connect to can_rx_bus of external driver)
canbus_tx	out	CANbus transmit signal, connected to external driver
canbus_tx_ebl_n	out	External driver control signal

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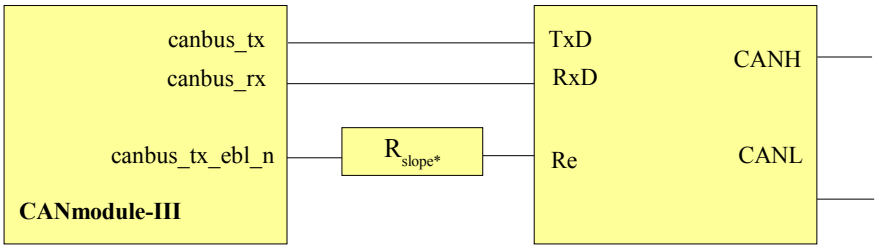
Standard CANbus transceiver chips can directly be connected to the CAN interface pins. The following figure shows how to connect an external Phillips CAN driver.



*) See specification of third party CAN transceiver for definition of R_{slope}.

Figure 3: 3 Pin CANbus Interface

To minimize the number of pins used, a two port configuration is also possible:

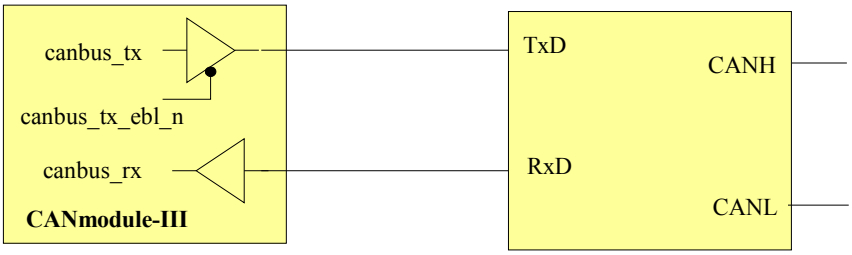


Figure 4: 2 Pin CANbus Interface

2.5 SRAM Port

A synchronous on-chip SRAM is used to store Rx and Tx messages. The SRAM is external to the core so technology adaption and test strategies don't require any modification of the core logic. The following diagram shows how to connect the core to the SRAM module:

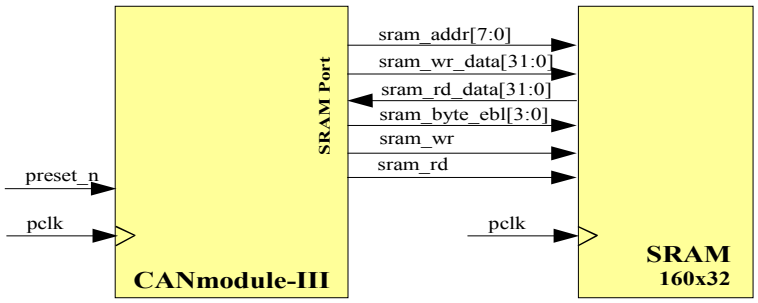


Figure 5: SRAM Connection

SRAM Interface Pins

Pin Name	*Type*	*Description*
sram_addr[7:0]	out	SRAM address bus
sram_wr_data[31:0]	in	Write data bus
sram_rd_data[31:0]	out	Read data bus
sram_byte_ebl[3:0]	out	Byte valid indicator, active high [0]: Byte valid for sram_wr_data[7:0] [1]: Byte valid for sram_wr_data[15:8] [2]: Byte valid for sram_wr_data[23:16] [3]: Byte valid for sram_wr_data[31:24]
sram_wr	out	Write enable, active high
sram_rd	out	Read enable, active high

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3 Programmer's Model

The table below shows the entire memory map of the CANmodule-III function. All registers are 32-bit wide. Following nomenclature is used to differentiate different bus access:

r : Data read back operation. Read back of configuration registers
R : Read operation
W : Write operation

Default value for all register if not otherwise noted is 0x00.

3.1 Memory map of all internal registers:

Address	*Type*	*Description*
0x000	R/W	Interrupt Control
0x008	R/W	Buffer Status Indicators
0x00C	R/W	Error Status Indicators
0x010	R/W	CAN Operating Mode
0x014	r/W	CAN Configuration
0x020	r/W	TxMessage0 Buffer
0x030	r/W	TxMessage1 Buffer
0x040	r/W	TxMessage2 Buffer
0x050	r/W	TxMessage3 Buffer
0x060	r/W	TxMessage4 Buffer
0x070	r/W	TxMessage5 Buffer
0x080	r/W	TxMessage6 Buffer
0x090	r/W	TxMessage7 Buffer
0x0A0	R/W	RxMessage0 Buffer
0x0C0	R/W	RxMessage1 Buffer
0x0E0	R/W	RxMessage2 Buffer
0x100	R/W	RxMessage3 Buffer
0x120	R/W	RxMessage4 Buffer
0x140	R/W	RxMessage5 Buffer

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Address	Type	Description
0x160	R/W	RxMessage6 Buffer
0x180	R/W	RxMessage7 Buffer
0x1A0	R/W	RxMessage8 Buffer
0x1C0	R/W	RxMessage9 Buffer
0x1E0	R/W	RxMessage10 Buffer
0x200	R/W	RxMessage11 Buffer
0x220	R/W	RxMessage12 Buffer
0x240	R/W	RxMessage13 Buffer
0x260	R/W	RxMessage14 Buffer
0x280	R/W	RxMessage15 Buffer

3.2 Internal Register Description

This paragraph shows all internal registers and describes how the CANmodule-III can be used and programmed.

3.2.1 Interrupt Controller

The interrupt controller contains an interrupt status and an interrupt enable register. The interrupt status register stores internal interrupt events. Once a bit is set it remains set until it is cleared by writing a '1' to it. The interrupt enable register has no effect on the interrupt status register.

The interrupt enable register controls which particular bits from the interrupt status register are used to assert the interrupt output int_n. int_n is asserted if a particular interrupt status bit and the respective enable bit are set.

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Address	Name	R/W	Comment
0x000	IntStatus	R/W	Interrupt Status Register. A pending interrupt is indicated that its respective flag is set to '1'. To acknowledge an interrupt, set its flag to '1'. [12]: rx_msg [11]: tx_msg [10]: rx_msg_loss [9]: bus_off [8]: crc_err [7]: form_err [6]: ack_err [5]: stuff_errr [4]: bit_err [3]: ovr_load [2]: arb_loss [1]: N/A [0]: N/A
0x004	IntEbl	r/W	A particular interrupt source is enabled by setting its respective flag to '1'. [12]: rx_msg [11]: tx_msg [10]: rx_msg_loss [9]: bus_off [8]: crc_err [7]: form_err [6]: ack_err [5]: stuff_errr [4]: bit_err [3]: ovr_load [2]: arb_loss [1]: N/A [0]: int_ebl, global interrupt enable flag '0': All interrupts are disabled '1': Enabled interrupt sources are available

Explanation of interrupt sources:

rx_msg:	Indicates that a message was received.
tx_msg:	Indicates that a message was sent.
rx_msg_loss:	Is set when a new message arrives but the RxMessage flag MsgAv is set.
bus_off:	The CAN has reached the bus off state.
crc_err:	A CAN CRC error was detected.

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form_err: A CAN message format error was detected.

ack_err: An CAN message acknowledge error was detected.

stuff_err: A bit stuffing error was detected.

bit_err: A bit error was detected.

ovr_load: An overload frame was received.

arb_loss: The arbitration was lost while sending a message.

3.2.2 Buffer Status Indicators

These status indicators bundle the respective flags from all RxMessage and TxMessage buffers.

Address	*Name*	*R/W*	*Comment*
0x008	BufferStatus	R	RxMessage and TxMessage Buffer Status [23]: TxMessage7 - TxReq pending .. [16]: TxMessage0 - TxReq pending [15]: RxMessage15 – MsgAv .. [0]: RxMessage0 - MsgAv

Note: All flags are read only! E.g., to acknowledge a MsgAv flag, the CPU has to write to the respective RxMessage buffer.

3.2.3 Error Status Indicators

Status indicators are provided to report the CAN controller error state, receive error count and transmit error count. Special flags to report error counter values equal to or in excess of 96 errors are available to indicate heavily disturbed bus situations.

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Address	Name	R/W	Comment
0x00C	ErrorStatus	R	CAN Error Status [19]: rxgte96 The Rx error counter is greater or equal 96_{dec} [18]: txgte96 The Tx error counter is greater or equal 96_{dec} [17:16]: error_state[1:0] The error state of the CAN node: "00": error active (normal operation) "01": error passive "1x": bus off [15:8]: rx_err_cnt[7:0] The receiver error counter according to the CAN standard. When in bus-off state, this counter is used to count the idle periods. [7:0]: tx_err_cnt[7:0] The transmitter error counter according to the CAN standard. When it is greater than 255_{dec}, it is fixed at 255_{dec}.

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3.2.4 Operating Modes

The CANmodule-III can be used in different operating modes. By disabling transmitting data, it is possible to use the CAN in listen only mode, enabling features such as automatic bit rate detection.

Before starting the CAN controller, all the CAN configuration registers have to be set according to the target application.

Address	*Name*	*R/W*	*Comment*
0x010	Command	R/W	CAN Command Register [1]: Listen only mode: 0': Active 1': CAN listen only: The output is held at 'R' level. The CANmodule-III is only listening [0]: Run/Stop mode: '0': Sets the CAN controller into stop mode. Returns '0' when stopped. '1': Sets the CAN controller into run mode. Returns '1' when running.

3.2.5 CAN Configuration Register

The CANmodule-III has to be configured prior to its use. Following registers define the effective CAN data rate[1], CAN data synchronization, and message buffer arbitration. These registers have to be set before the CAN controller is started.

1 Additional information on the CAN data rate settings using time segment 1 (tseg1), time segment 2 (tseg2), and bit rate are given in chapter 4.

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Address	Name	R/W	Comment
0x014	Config	R/W	CAN Configuration [30:16]: cfg_bitrate[14:0]: Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles [12]: cfg_arbiter: Transmit buffer arbiter '0': Round robin arbitration '1': Fixed priority arbitration [11:8]: cfg_tseg1: Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. [7:5]: cfg_tseg2: Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. [4]: auto_restart '0': After bus-off, the CAN must be restarted 'by hand'. This is the recommended setting. '1': After bus-off, the CAN is restarting automatically after 128 groups of 11 recessive bits [3:2]: cfg_sjw: Synchronization jump width - 1 sjw ≤ tseg1 and sjw ≤ tseg2

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Address	Name	R/W	Comment
0x014	Config *continued*	R/W	CAN Configuration (continued) [1]: sampling_mode: CAN bus bit sampling '0': One sampling point is used in the receiver path '1': 3 sampling points with majority decision are used [0]:edge_mode: CAN bus synchronization logic '0': Edge from 'R' to 'D' is used for synchronization '1': Both edges are used

3.2.6 Tx Message Registers

Eight transmit message holding buffers are provided. An internal priority arbiter selects the message according to the chosen arbitration scheme. Upon transmission of a message or message arbitration loss, the priority arbiter re-evaluates the message priority of the next message.

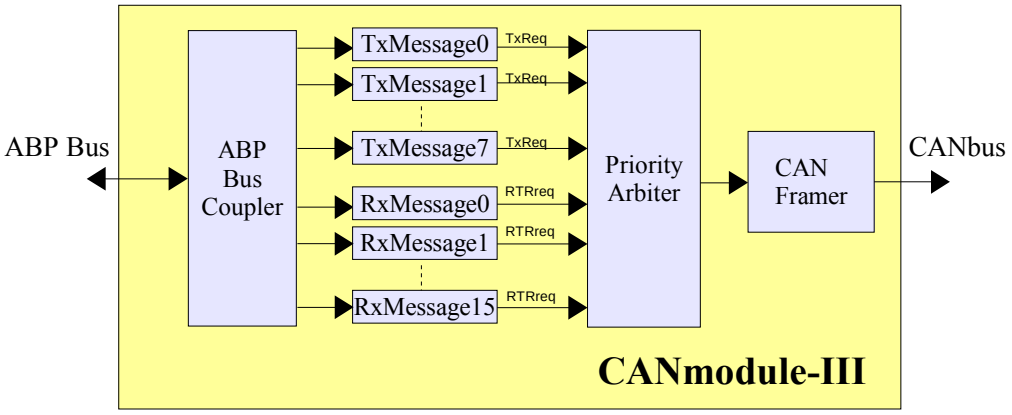

Figure 6: Message Arbitration

Message Arbitration

The priority arbiter supports round robin and fixed priority arbitration. The arbitration mode is selected using the configuration register.

- Round Robin: Buffers are served in a defined order: 0-1-2..7-0-1... A particular buffer is only selected if its TxReq flag is set. This scheme guarantees that all buffers receive the same probability to send a message.
- Fixed Priority: Buffer 0 has the highest priority. This way it is possible to designate buffer 0 as the buffer for error messages and it is guaranteed that they are sent first.

Note: RTR message requests are served before TxMessage buffers are handled. E.g., RTRreq0, ... RTRreq15, TxMessage0, TxMessage1, ... TxMessage7

Register Mapping Transmit Buffers

The register mapping of the transmit buffers is shown in the table below.

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Address	Name	R/W	Comment
0x020	TxMessage0. Control	r/W	TxMessage0 Buffer: Control Flags [23]: WPN, Write Protect Not[2] '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. This bit is always zero for readback [21]: RTR, Remote Bit '0': This is a standard message '1': This is an RTR message [20]: IDE, Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message [19:16]: DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes
0x020	TxMessage0. Control *continued*	r/W	TxMessage0 Buffer: Control Flags [3]: WPN: Write protect not. '0': Bit [2] remains unchanged '1': Bit [2] is modified, default. This bit is always zero for readback [2]: TxIntEbl, Tx Interrupt Enable '0': Interrupt disabled '1': Interrupt enabled, successful message transmission sets the TxMsg flag in the interrupt controller.

2 Using the WPN flag enables simple retransmission of the same message by only having to set the TRX flag without taking care of the special flags

1 Using the WPN flag enables simple retransmission of the same message by only having to set the TRX flag without taking care of the special flags

Address	Name	R/W	Comment
0x020	TxMessage0. Command	R/W	TxMessage0 Buffer: Command Flags [23]: WPN, Write Protect Not[1] '0': default '1': prohibited [3]: WPN: Write Protect Not[1] '0': default '1': prohibited [1]: TxAbort, Transmit Abort Request '0': idle '1': Requests removal of a pending message. The message is removed the next time an arbitration loss happened. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time [0]: TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request[3] Read: '0': TxReq completed '1': TxReq pending
0x024	TxMessage0. ID	r/W	TxMessage0 Buffer: Identifier [31:3]: ID[28:0] [2:0]: N/A
0x028	TxMessage0. DataHigh	r/W	TxMessage0 Buffer: Data high[4] [31:0]: Data[63:32]
0x02C	TxMessage0. DataLow	r/W	TxMessage0 Buffer: Data low[3] [31:0]: Data[31:0]
0x030-0x03C	TxMessage1 Buffer, see TxMessage0 Buffer for description		
0x040-0x04C	TxMessage2 Buffer, see TxMessage0 Buffer for description		

3 The Tx message buffer must not be changed while TxReq is '1'!

4 Byte 1 is Data[63:56], Byte 2 is Data[55:48], etc.

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Address	Name	R/W	Comment
0x050-0x05C	TxMessage3 Buffer, see TxMessage0 Buffer for description		
0x060-0x06C	TxMessage4 Buffer, see TxMessage0 Buffer for description		
0x070-0x07C	TxMessage5 Buffer, see TxMessage0 Buffer for description		
0x080-0x08C	TxMessage6 Buffer, see TxMessage0 Buffer for description		
0x090-0x09C	TxMessage7 Buffer, see TxMessage0 Buffer for description		

Procedure for sending a message

- Write message into an empty transmit message holding buffer. An empty buffer is indicated by TxReq is equal to *zero*.
- Request transmission by setting the respective TxReq flag to *one*.
- The TxReq flag remains set as long as the message transmit request is pending. The content of the message buffer must not be changed while the TxReq flag is set!
- The internal message priority arbiter selects the message according to the chosen arbitration scheme
- Once the message was transmitted, the TxReq flag is set to *zero* and the TxMsg interrupt status bit is asserted.

Procedure for removing a message from a transmit holding register

A message can be removed from a transmit holding buffer by asserting the TxAbort flag. Use following procedure to remove the contents of a particular TxMessage buffer:

- Set TxAbort to *one* to request the message removal.

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- This flag remains set as long as the message abort request is pending. It is cleared when either the message won arbitration (TxMsg interrupt active) or the message was removed (TxMsg interrupt inactive)

3.2.7 Rx Message Buffers

The CANmodule-III provides 16 individual receive message buffers. Each one has its own message filter mask. Automatic reply to RTR messages is supported.

If a message is accepted in a receive buffer, its MsgAv flag is set. The message remains valid as long as MsgAv flag is set. The host CPU has to reset the MsgAv flag to enable receipt of a new message.

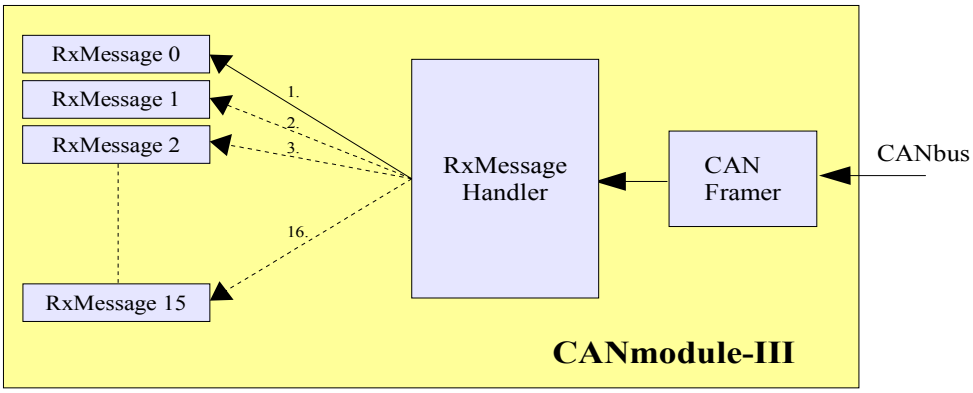

Figure 7: Receive Message Handler

Rx Message Processing

After receipt of a new message, the RxMessageHandler searches all receive buffer starting from RxMessage0 until it finds a valid buffer.

A valid buffer is indicated by:

- Receive buffer is enabled indicated by RxBufferEbl = '1'
- Acceptance Filter of receive buffer matches incoming message

If the RxMessageHandler finds a valid buffer that is empty, then the message is stored and the MsgAv flag of this buffer is set to '1'. If the RxIntEbl flag is set, than

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the RxMsg flag of the interrupt controller is asserted. If the receive buffer already contains a message indicated by MsgAv = '1' and the Link Flag is not set, then the RxMsgLoss interrupt flag is asserted.

If an incoming message has its RTR flag set and the RTRreply flag of the matching buffer is set, then the message is not stored but an RTR auto-reply request is issued. See paragraph 'RTR Auto-Reply' for more details.

Acceptance Filter

Each receive buffer has its own acceptance filter that is used to filter incoming messages. An acceptance filter consists of Acceptance Mask Register (AMR) and Acceptance Code Register (ACR) pair. The AMR defines which bits of the incoming CAN message have to match the respective ACR bits.

Following message fields are covered:

- ID
- IDE
- RTR
- Data byte 1 and data byte 2 (DATA[63:56])[5]

The acceptance mask register (AMR) defines whether the incoming bit is checked against the acceptance code register (ACR).

AMR: '0': The incoming bit is checked against the respective ACR. The message is not accepted when the incoming bit doesn't match respective ACR flag

'1': The incoming bit is don't care

Example:

The following example shows the acceptance register settings used to support receipt of a CANopen TPDO1 (Transmit Process Data Object) message. In CANopen, a widely used CAN Higher Level Protocol (HLP), the ID bits are used to select the message type. The bit assignment is shown in following table:

CANopen Identifier										
10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

5 Some CAN High Level Protocols such as SDS or Device Net carry additional protocol related information in the first or first two data bytes that are used for message acceptance and selection. Having the capability to filter on these fields provides a more efficient implementation of the protocol stack running on the CPU.

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CANopen Identifier	
Function Code	Node-ID

Identifier fields:

- Function Code: The function code for a TDPO1 message is 3h
- Node-ID: In our example, we use 02h as the Node ID
- IDE = '0', CANopen uses the short format message
- RTR = '0', this is a regular message

To accept this message, the acceptance filter settings would look like

AMR settings:

- ID[28:18] = 0
- ID[17:0] = all ones
- IDE = 0
- RTR = 0
- DATA[63:56] = all ones

ACR settings:

- ID[28:18] = 182h
- ID[17:0] = don't care
- IDE = 0
- RTR = 0
- DATA[63:56] = don't care

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RTR Auto-Reply

The CANmodule-III supports automatic answering of RTR message requests. All 16 receive buffers support this feature. If an RTR message is accepted in a receive buffer where the RTRreply flag is set, then this buffer automatically replies to this message with the content of this receive buffer. The RTRreply_pending flag is set when the RTR message request is received. It is reset when the message was sent or when the message buffer is disabled. To abort a pending RTRreply message, use the RTRabort command.

RxBuffer Linking

Several receive buffers may be linked together to form a receive buffer array which acts almost like a receive FIFO.

Requirements:

- All buffers of the same array must have the same message filter setting (AMR and ACR are identical)
- The last buffer of an array may not have its link flag set

When a receive buffer already contains a message (MsgAv='1') and a new message arrives for this buffer, then this message would be discarded (RxMsgLoss Interrupt). To avoid this situation several receive buffers can be linked together. When the CANmodule-III receives a new message, the RxMessage handler searches for a valid receive buffer. If one is found that is already full (MsgAv='1') and the link flag is set (BufferLink='1'), the search for a valid receive buffer is continued. If no other buffer is found, than the RxMsgLoss interrupt is set anyway.

It is possible to build several message arrays. Each of these arrays must use the same AMR and ACR.

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Register Mapping Receive Buffers

The register mapping of the receive buffers is shown in the table below.

Address	*Name*	*R/W*	*Comment*
0x0A0	RxMessage0. Command	R/W	RxMessage0: Command/Status [23]: WPNH, Write Protect Not High '0': default '1': prohibited [7]: WPNL, Write Protect Not Low '0': default '1': prohibited [2]: RTRabort, RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. [1]: RTReply_pending '0': No RTR reply request pending '1': RTR reply request pending [0]: MsgAv, Message Available Read: '0': No new message available '1': New message available Write: '0': idle '1': Acknowledges receipt of new message [1]

1 Before acknowledging receipt of a new message, the message content must be copied into system memory. Acknowledging a message clears the MsgAv flag.

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Address	Name	R/W	Comment
0x0A0	RxMessage0. Control	R/W	RxMessage0: Control [23]: WPNH, Write Protect Not High '0': Bit [21:16] remain unchanged '1': Bit [21:16] are modified, default. This bit is always zero for readback [21]: RTR, Remote Bit '1': This is an RTR message '0': This is a regular message [20]: IDE, Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message [19:16]: DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is not valid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes [7]: WPNL, Write Protect Not Low '0': Bits [6:3] remain unchanged '1': Bits [6:3] are modified, default. This bit is always zero for readback [6]: Link Flag ‘0’: This buffer is not linked to the next ‘1’: This buffer is linked with next buffer [5]: RxIntEbl, Receive Interrupt Enable ‘0’: Interrupt generation is disabled '1': Interrupt generation is enabled [4]: RTRreply, automatic message reply upon receipt of an RTR message ‘0’: Automatic RTR message handling disabled ‘1’: Automatic RTR message handling enabled [3]: Buffer Enable ‘0’: Buffer is disabled ‘1’: Buffer is enabled

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Address	Name	R/W	Comment
0x0A4	RxMessage0. ID	R/W	RxMessage: Identifier [31:3]: ID[28:0] [2:0]: zeros
0x0A8	RxMessage0. DataHigh	R/W	RxMessage Data high [31:0]: Data[63:32]
0x0AC	RxMessage0. DataLow	R/W	RxMessage Data low [31:0]: Data[31:0]
0x0B0	RxMessage0. AMR	r/W	Acceptance Mask Register [31:3]: Identifier [2]: IDE [1]: RTR [0]: N/A
0x0B4	RxMessage0. ACR	r/W	Acceptance Code Register [31:3]: Identifier [2]:IDE [1]: RTR [0]:N/A
0x0B8	RxMessage0. AMR_Data	r/W	Acceptance Mask Register – Data [15:0]: Data[63:48]
0x0BC	RxMessage0. ACR_Data	r/W	Acceptance Code Register – Data [15:0]: Data[63:48]
0x0C0-0x0DC	RxMessage1 Buffer, see RxMessage0 Buffer for description		
0x0E0-0x0FC	RxMessage2 Buffer, see RxMessage0 Buffer for description		
0x100-0x11C	RxMessage3 Buffer, see RxMessage0 Buffer for description		
0x120-0x13C	RxMessage4 Buffer, see RxMessage0 Buffer for description		
0x140-0x15C	RxMessage5 Buffer, see RxMessage0 Buffer for description		
0x160-0x17C	RxMessage6 Buffer, see RxMessage0 Buffer for description		
0x180-019C	RxMessage7 Buffer, see RxMessage0 Buffer for description		

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Address	Name	R/W	Comment
0x1A0-0x1BC	RxMessage8 Buffer, see RxMessage0 Buffer for description		
0x1C0-0x1DC	RxMessage9 Buffer, see RxMessage0 Buffer for description		
0x1E0-0x1FC	RxMessage10 Buffer, see RxMessage0 Buffer for description		
0x200-0x21C	RxMessage11 Buffer, see RxMessage0 Buffer for description		
0x220-0x23C	RxMessage12 Buffer, see RxMessage0 Buffer for description		
0x240-0x25C	RxMessage13 Buffer, see RxMessage0 Buffer for description		
0x260-0x27C	RxMessage14 Buffer, see RxMessage0 Buffer for description		
0x280-0x29C	RxMessage15 Buffer, see RxMessage0 Buffer for description		

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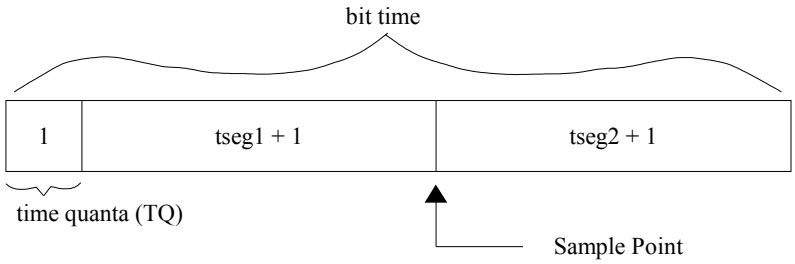
4 Configuring The CAN Controller

4.1 Setting proper bit rate, tseg1 and tseg2

Following relations exist for bit time, time quanta, time segments 1/2 and the data sampling point.



$$bittime = (1 + (tseg1 + 1) + (tseg2 + 1)) * timequanta$$

$$timequanta = \frac{bitrate + 1}{f_{clk}}$$

Figure 8: Bit-rate and bit-time settings

E.g.,

for 1 Mbps with fclk = 8 Mhz, set bitrate = 0, tseg1 = 3 and tseg2 = 2

for 1 Mbps with fclk = 40 Mhz, set bitrate = 4, tseg1 = 3 and tseg2 = 2

Please observe following conditions for setting tseg1 and tseg2:

- tseg1=0 or tseg1=1 are not allowed
- tseg2=0 is not allowed; tseg2=1 is only allowed in direct sampling mode.

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