INICORE System-on-Chip from Spec to Silicon

Optimized for Actel

WDmodule

Description

The WDmodule is part of Inicore's IPmodule family. A watchdog is used in systems to prevent system lockup due to software or hardware failures.

For normal operation, the timeout counter has to be reset by the CPU in a regular interval. Depending on the watchdog configuration, the watchdog asserts the reset_req and int_req outputs upon expiration of the timeout counters.

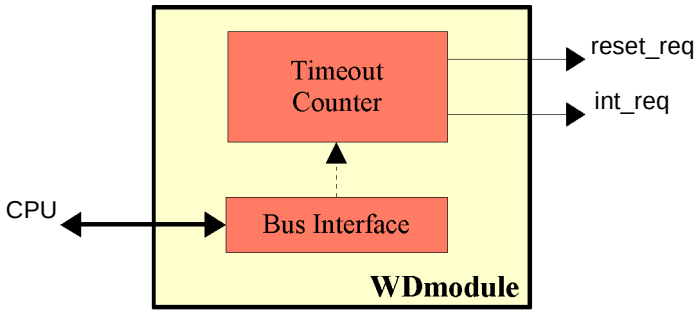

Figure 1: Block diagram

All configuration registers are protected by a special lock key to avoid unintended reconfiguration of the watchdog.

The timeout interval can be configured over a wide range:

- min: 65536 system clock cycles
- max: 67'108'864 system clock cycles

Using a system clock of 40MHz, this results in a timeout window of 1.6ms – 1.67s.

Features

- Two timeout outputs
- Configurable timeout interval
- Configuration register protected with lock key
- Timeout interval with 40Mhz clock:
  - min: 1.6ms
  - max: 1.67s
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
  - CPU readback enable
  - Selectable lock key and reset key values
  - CPU bus width

Applications

- Industrial control
- System-on-Chip
- Peripheral Logic
- Embedded Systems

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC PLUS	APA300			305		4%
Axcelerator	AX500-3	41	70			1%
SXA	SX32A-3	41	72			2%
eX	EX256	41	72			15%

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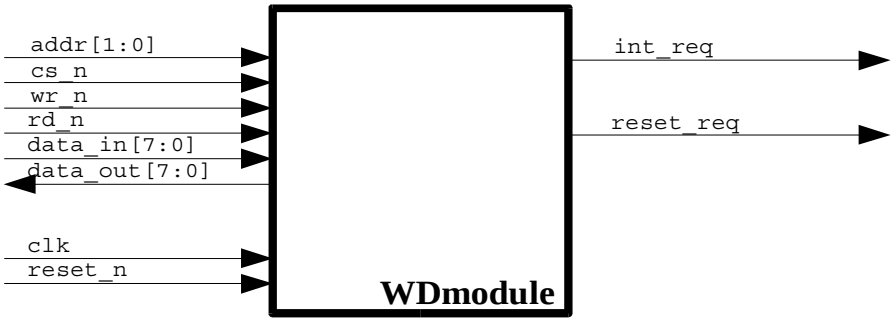

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[1:0]	in	Address bus input
data_in[7:0]	in	Data bus input
data_out [7:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
System Port		
int_req	out	Interrupt request
reset_req	out	Reset request

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. Synthesis options are included to use the core in 8, 16 and 32-bit systems.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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