Optimized for

SPIMmodule

Description

The SPIMmodule is part of Inicore's IPmodule family. The serial peripheral interface (SPI) protocol is often used to connect peripheral devices to a CPU. Several slave devices can be connected to the same bus. Since it is a serial bus, the pin count is low.

The SPIMmodule is a single master controller and uses a message queue based architecture. A message consists of the command, transmit data and receive data field. The command field defines the length of the SPI access (1-32 bits, or continued in the next command), the selected slave device, the SS to SCK delay and the delay after transfer control. Using the queue, several SPI commands can be executed without CPU interaction.

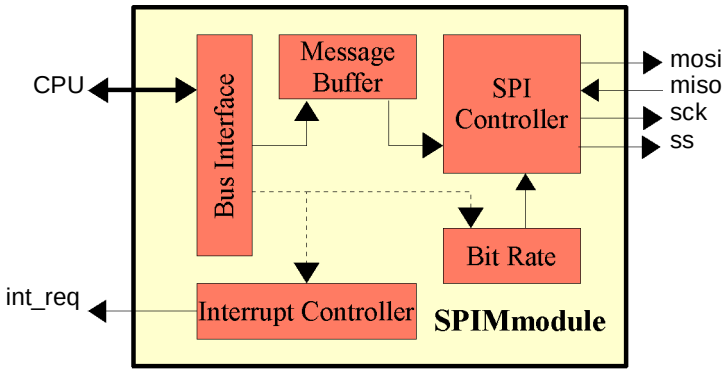

Figure 1: Block diagram

A range of messages can be selected to be sent by the SPI controller. There is a wrap mode to enable continuously sending the same messages.

The SPI controller supports all standard modes. The clock phase and clock polarity can be configured as well as the bit rate and slave select polarity.

Features

- Standard SPI single master
- Full duplex operation
- Programmable frame length, transfer delay, ss to sck delay, slave select
- Continous re-transfer mode
- Supports all SPI modes: configurable clock polarity and phase
- Message queue buffer
- Programmable bitrate
- Local interrupt controller
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
  - CPU readback enable
  - Number of slave selects
  - Message queue depth

Applications

- Industrial control
- System-on-Chip
- Peripheral Logic
- Embedded Systems

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC[PLUS]	APA150			1045		17%
Axcelerator	AX500-3	306	309			8%
SXA	SX16A-3	307	316			43%

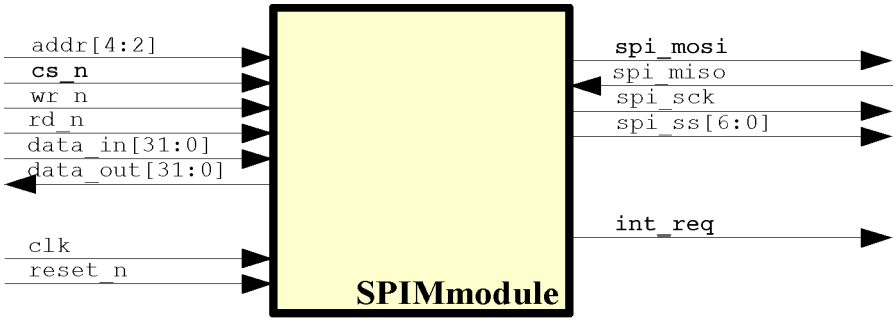

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[4:2]	in	Address bus input
data_in[31:0]	in	Data bus input
data_out [31:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
int_req	out	Interrupt request
Serial Interface		
spi_mosi	out	SPI master output slave input
spi_miso	in	SPI master input slave output
spi_sck	out	SPI serial clock
spi_ss[6:0]	out	SPI slave select

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. The depth of the message queue as well as the number of slave devices can be selected prior to synthesis. The core supports replacing the register files used for the message buffer with on-chip memories.

Using a separate APB wrapper, the core can be easily integrated into ARM based systems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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