INICORE
System-on-Chip from Spec to Silicon

Optimized for

Actel

PCIXarbiter

Description

In PCI-X systems, a central controller is used to manage bus ownership. This controller, called arbiter, selects the next master for bus ownership.

The PCIXarbiter core implements this function. It is compliant with the PCI-X Addendum to the PCI Local Bus Specification, revision 1.0a. This core supports up to 5 PCI-X bus masters. Round robin arbitration is used to select the next master. This core supports PCI-X only systems. It may not be used in mixed PCI-PCI-X systems.

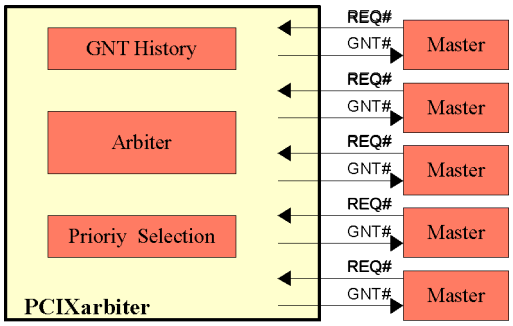

Figure 1: System diagram

Arbitration Scheme

The arbiter uses a round-robin arbitration to select the next master. After reset, master 0 is granted default master. If all masters request the bus at the same time, the order of which the bus grant asserted is 0 => 1 => 2 => 3 => 4 => 0 ...

Features

- PCI-X rev 1.0a compliant
- Supports 66/100/133MHz
- Fair arbitration using round robin
- Supports up to 5 masters
- Bus parking on latest selected master
- Hidden arbitration
- Observes arbitration timeout
- Limited to PCIX only systems
- Full synchronous design

References

- PCI-X rev 1.0a
- PCI specification

Applications

- Telecom
- Datacom
- Embedded systems

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
Axcelerator	AX500-3	94	47			5%
SXA	SX72A-3	96	47			2%

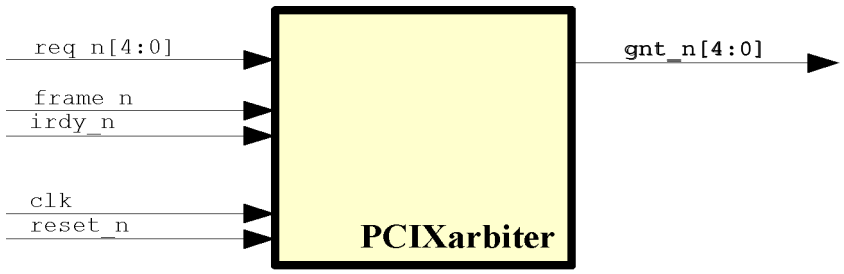

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
PCI-X Interface		
req_n[4:0]	in	PCI-X REQ#
gnt_n[4:0]	out	PXI-X GNT#
frame_n	in	PCI-X FRAME#
irdy_n	in	PCI-X IRDY#

Operation

Bus Parking

To prevent bus floating, always one master has to be granted bus ownership. If no master request is pending, the arbiter parks the bus on the last selected master by keeping its respective GNT# asserted.

Device Arbitration Timeout

A master requesting the bus must initiate a transaction upon having its grant asserted. If the bus remains idle for more than 15 clock cycles, the arbiter assumes the selected master 'broken'. A broken master can reactivate himself again by removing its bus request and reasserting it again. Broken masters are removed from the regular arbitration process.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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