

GPIOmodule

Description

The GPIOmodule is part of Inicore's IPmodule family. This general purpose input/output controller provides some unique features that eases system integration and use.

Each GPIO port can be configured for input, output or bypass mode. All output data can be set in one access. Single or multiples bits can be set or cleared independently. Every GPIO port can serve as an interrupt source and has its own configuration options:

- Level sensitive, single edge triggered or level change
- Active high or low respectively rising edge or falling edge
- Individual interrupt enable register and status flags

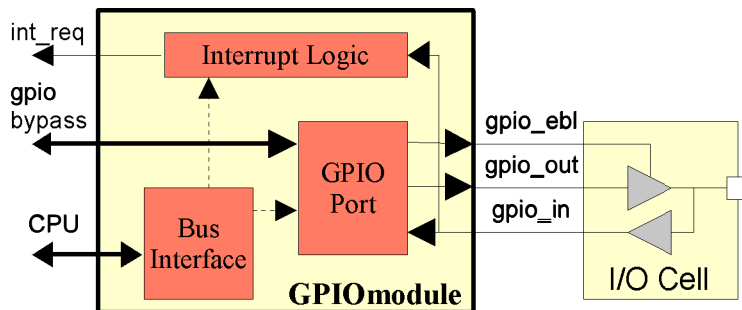


Figure 1: Block diagram

The core provides several synthesis options to ease the system integration and minimize the gate count:

- Selectable CPU bus width: default options are 8/16/32-bit
- Selectable number of GPIO ports
- CPU readback enable

Features

- Up to 32 ports
- Each port can be input, output or bypass
- Data set or bitwise set and clear control
- Input data synchronization
- Flexible interrupt generation for each GPIO pin
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
 - CPU readback enable
 - CPU bus width
 - Number of ports

Applications

- Industrial control
- System-on-Chip
- Peripheral Logic
- Embedded Systems

Utilization Table Optimized for Actel Devices

Family	Device - (speed grade)	Utilization				
		s-mod	c-mod	Tiles	RAM	Total
ProASIC ^{PLUS}	APA150			393		5%
Axcelerator	AX500-3	88	110			2%
SXA	SX32A-3	88	116			3%
eX	EX256	88	116			27%

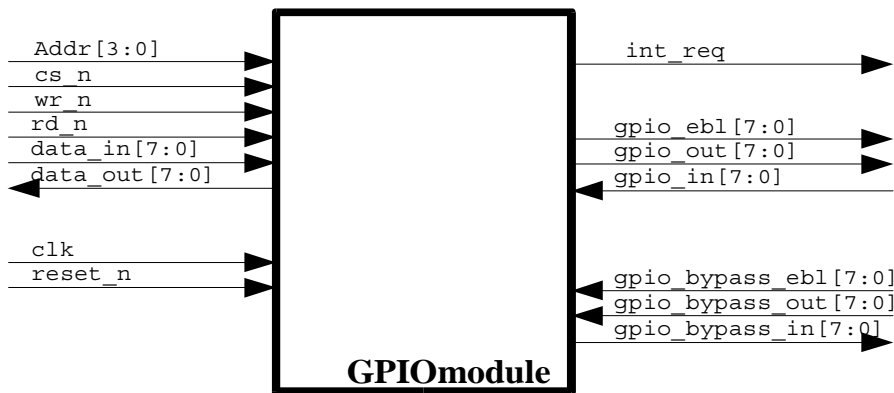


Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[3:0]	in	Address bus input
data_in[7:0]	in	Data bus input
data_out [7:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
int_req	out	System interrupt request
IO Port		
gpio_ebl[7:0]	out	GPIO output pin enable
gpio_in[7:0]	in	GPIO input
gpio_out[7:0]	out	GPIO output
Bypass Port		
gpio_bypass_ebl[7:0]	in	Bypass GPIO output pin enable
gpio_bypass_in[7:0]	out	Bypass GPIO input
gpio_bypass_out[7:0]	in	Bypass GPIO output

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. Synthesis options are included to use the core in 8, 16 and 32-bit systems.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- ◆ FPGA and ASIC Design
- ◆ Easy-to-use IP Cores
- ◆ System-on-Chip Solutions
- ◆ Consulting Services
- ◆ ASIC to FPGA Migration
- ◆ Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

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