INICORE
System-on-Chip from Spec to Silicon

Optimized for

Actel

CANmodule-III

Description

The CANmodule-III is part of Inicore's IPmodule family. The controller area network (CAN) bus, originally developed for the car industry, is a fast, reliable and cost-effective data bus for multi-master and real-time applications. In addition to automotive applications, it is in wide use in applications such as factory automation, machine control, building automation, maritime, medical, railway and avionics.

CANmodule-III is a full functional CAN controller that uses the concept of message objects. All message objects are stored in a shared on-chip SRAM. The core contains a CAN2.0B compliant bus framer, receive and transmit message handlers, the memory arbiter, an interrupt controller and the system bus interface.

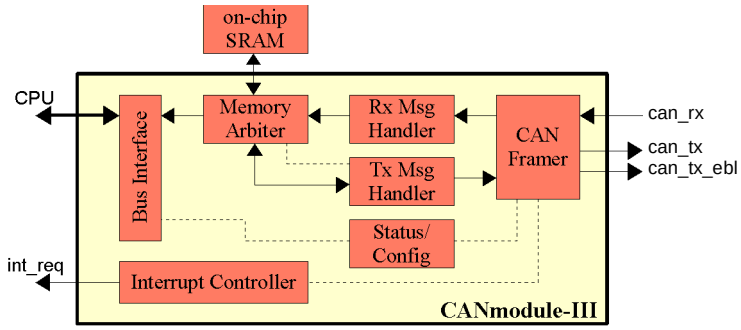

Figure 1: Block diagram

This CANmodule-III has 16 separate receive message objects. Each one has its own acceptance filter with code and mask bits covering the entire ID, IDE, RTR and the first two Data fields. Several message objects can be linked together to build a receive queue. Each object can be configured to automatically handle RTR request and eliminating CPU overhead.

On the transmit side, eight message objects can be stored in the SRAM memory. The transmit message handler selects the next message based either on a fixed or round robin priority scheme.

The CAN framer contains the complete data link layer, including the framer, transmit and receive control, error handling, error reporting and bit synchronization.

Features

- Full CAN2.0B compliant
- Maximum baudrate 1Mbps
- 16 receive message objects
  - Acceptance filters
  - RTR auto-replay handlers
  - Buffer linking for Rx queue
- Enhanced for DeviceNet
- 8 transmit message objects
- Programmable Tx priority
- Local interrupt controller
- Listen only mode
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
  - CPU readback enable
  - CPU bus width

Applications

- Factory automation
- Machine control
- Automotive
- Avionics and Aerospace
- Building automation

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC[PLUS]	APA150			5450	4	89%
Axcelerator	AX500-3	1106	2125		1	40%
SXA	SX72A-3	1107	2236		*external*	55%

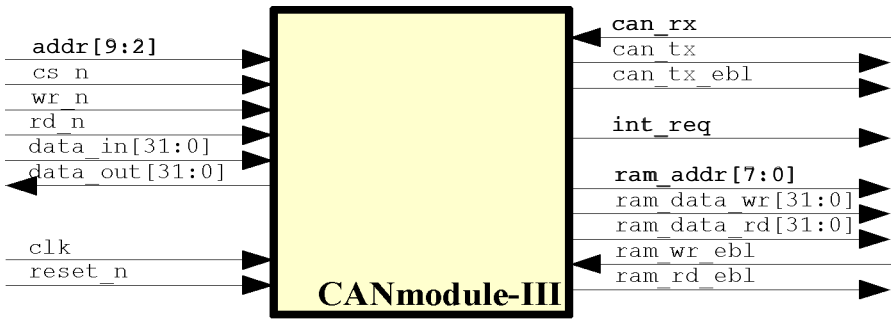

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[9:2]	in	Address bus input
data_in[31:0]	in	Data bus input
data_out [31:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
int_req	out	Interrupt request
on-chip SRAM		
ram_data_wr[31:0]	out	RAM data output
ram_data_rd[31:0]	in	RAM data input
ram_addr[7:0]	out	RAM address
ram_wr_ebl	out	RAM write enable
ram_rd_ebl	out	RAM read enable
CANbus		
can_rx	out	CANbus receive signal from extern driver
can_tx	in	CANbus transmit signal to extern driver
can_tx_ebl	out	CANbus transmit enable for external driver

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path.

Using a separate APB wrapper, the core can be easily integrated into ARM based systems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

51215.71.01 Dec/2002