INICORE
System-on-Chip from Spec to Silicon

Optimized for

Actel CompanionCore

CANmodule-IIx

Description

The CANmodule-IIx is part of Inicore's IPmodule family. The controller area network (CAN) bus, originally developed for the car industry, is a fast, reliable and cost-effective data bus for multi-master and real-time applications. In addition to automotive applications, it is in wide use in applications such as factory automation, machine control, building automation, maritime, medical, railway and avionics.

CANmodule-IIx is a full functional CAN controller that contains advanced message filtering, a Tx message FIFO, a high Tx-priority buffer and a Rx message FIFO. With advanced message filtering capabilities, this core helps to offload the CPU.

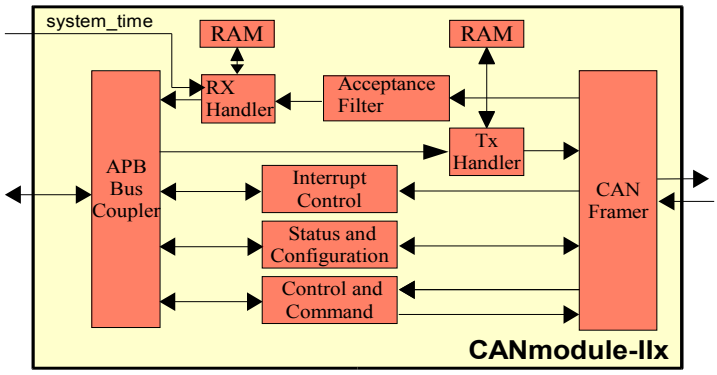

Figure 1 Block Diagram

There are three independent acceptance filters with their own code and mask registers. Each filters covers the entire ID, IDE, RTR, and enhanced DeviceNet support, the first two Data fields. The 32 message deep receive FIFO contains the entire message including acceptance filter match indicators.

The transmit FIFO can hold up to 16 messages. A high priority message can be placed in one separate buffer, which bypasses the Tx FIFO. The transmit site contains a local message priority arbiter.

Features

- Full CAN2.0B compliant
- Maximum baudrate 1Mbps
- 3 acceptance filters for ID, IDE, RTR and 2 Data fields
- Filters are user selectable
- Enhanced for DeviceNet
- 32 messages deep Rx FIFO *(default configuration)*
  - FIFO status indicator
  - System time stamp
- 16 messages deep Tx FIFO *(default configuration)*
  - 1 message buffer for high priority to bypass Tx FIFO
  - Message Arbiter
- Programmable interrupt controller
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
  - CPU readback enable
  - CPU bus width

Applications

- Factory automation
- Machine control
- Automotive
- Avionics and Aerospace
- Building automation

Sample Utilization and Performance Table Optimized for Actel Devices

Family	Device	Utilization				Performance
	- (speed grade)	s-mod	c-mod	RAM	Total	[MHz]
PA3e	A3PE600-2	321	1442	2	13%	30 / 83
ProASIC[PLUS]	APA450 STD	314	1691	4	16%	23 / 61
RTAX	RTAX1000S-1	344	941	2	7%	26 / 102
Axcelerator	AX500-3	344	941	2	16%	43 / 157

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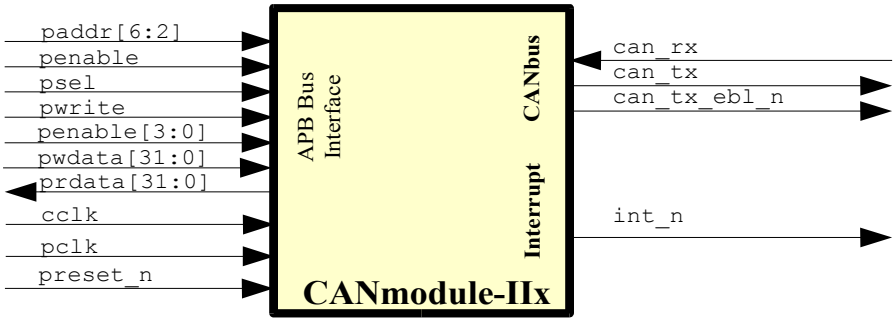

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
pclk	in	System clock
cclk	in	CAN clock
preset_n	in	Asynchronous system reset, active low
ABP Bus Interface		
psel	in	Module select signal
penable	in	Bus transfer enable signal
paddr[6:2]	in	Address bus
pwrite	in	Read/write signal '0': read operation '1': write operation
pwdata[31:0]	in	Write data bus
prdata[31:0]	out	Read data bus
int_n	out	Interrupt request, active low
CANbus		
can_rx_bus	in	CANbus receive signal from external driver
can_tx_bus	out	CANbus transmit signal connected to external driver
can_tx_ebl_n	out	External driver control signal

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the user has various options available: the register read-back path can be disabled, the configuration registers might be fixed, and Rx and Tx FIFO can be adapted to the system requirement. Furthermore the number of message filters can be individually selected, having the option of 0 or up to 3 CAN message filters available.

Using a separate APB wrapper, the core can be easily integrated into ARM based systems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

51220.71.03 Feb/2005